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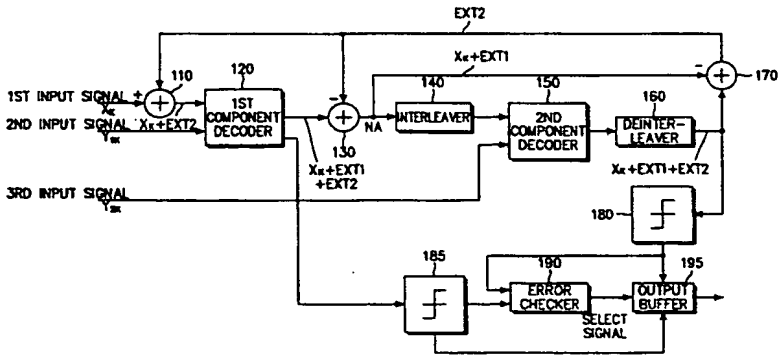

(57) Abstract

An iterative decoder and iterative decoding method. In the iterative decoder, a first adder has a first port for receiving information symbols and a second port; a first component decoder is coupled to the first adder, for receiving first parity symbols and decoding the information symbols using the first parity symbols and an output signal of the first adder; a first subtractor has a third port for receiving the output of the first component decoder, and a fourth port; an interleaver coupled to the output of the second adder, for interleaving the decoded information symbols received from the first component decoder; a second component decoder receives the output of the interleaver and second parity symbols and decodes the information symbols of the interleaver output using the received signals; a deinterleaver deinterleaves the output of the second component decoder; a third adder has a fifth port for receiving the output of the deinterleaver and a sixth port for receiving an inversed output of the second adder, the output of the third adder connected to the second port and an inverted output of the third adder connected to the fourth port; a hard decision device converts the decoded symbols received from the first component decoder to binary information bits; an error detector checks error in the binary information bits received from the hard decision device and generates a no error signal if no errors are detected; and an output buffer stores the binary information bits received from the hard decision device and outputs the stored binary information bits in response to the no error signal.

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AN ITERATIVE DECODER AND AN ITERATIVE DECODING METHOD FOR A COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a receiver in a communication system, and in particular, to a device and method for decoding an input signal.

2. Description of the Related Art

A transmitter in a radio communication system such as a satellite system, or a system using W-CDMA or CDMA 2000, can use a forward error correction code to ensure reliable data transmission. The receiver subjects the received data to iterative decoding, which feeds back the output of a component decoder to the input for decoding. The component decoder outputs not a hard-decision signal, like a high (+1) or low (-1) signal, but a soft value (e.g., 0.7684, –0.6432, . . .).

This interleaved sequence is input to a second component decoder, which decodes it. An iterative decoder is composed of at least two component decoders. An interleaver between the component decoders permutes the bit sequence of a frame output from a first component decoder. When the decoded interleaver signal is output for feedback to the first component decoder, a deinterleaver rearranges the bits of the decoded interleaved signal in their original order.

The turbo decoder is a preeminent example of iterative channel decoders. Iterative decoders, such as a turbo decoder, increase their error correction performance by many iterations of decoding.

In the conventional iterative decoding method, data decoding occurs a predetermined number of times without checking whether errors have been generated during the iterative decoding. Errors are checked by subjecting the deinterleaver output to hard decision decoding.

In the case of typical iterative decoding, however, the greatest decoding gain is generally obtained during the first two or three decodings, though this varies with the channel environment. In fact, error correction performance resulting from iterative decoding may rapidly drop after a number of decodings. Furthermore, after a certain number of iterative decodings, system resources, like power consumption and processing delay, are being dissipated for a marginal performance gain. For example, a certain number of iterative decodings can cause signal oscillations due to the feedback characteristics of the iterative decoder. In other words, perfectly error-corrected data can actually begin to generate errors as decoding is repeated.

The problem of the threshold number (the iteration number beyond which errors may be generated) of iterative decodings is overcome by appropriately picking the number of decoding iterations. If it can be determined that the probability that all errors have been correct is approximately 1, the iterative decoder need not decode the input signal any further. Whether decoding is completed can be determined in several ways. One of them is to check errors utilizing a CRC (Cyclic Redundancy Code) check of decoder output. Because the CRC check does not alter the information to be transmitted, it is impossible for the CRC check to generate errors in the decoded data. However, the challenging task for a system designer is to limit the additional processing delay that would be involved in performing an error check in the iterative decoding scheme. Therefore, a need exists for a device and method of limiting the number of iterations in an iterative decoder by performing an error check on the decoded data without incurring undue processing delay.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an iterative decoder and iterative decoding method for dynamically determining the appropriate number of decoding iterations of received data.

It is another object of the present invention to provide an iterative decoder

and iterative decoding method, in which the output of each component decoder is checked for the presence or absence of errors while decoding.

It is a third object of the present invention to provide an iterative decoder and iterative decoding method, in which the output of each component decoder is checked for the presence or absence of errors while decoding and which stops decoding immediately if no errors are detected.

It is a fourth object of the present invention to provide an iterative decoder and iterative decoding method, in which the processing delay is minimized during an error check of each component decoder output during decoding.

It is a fifth object of the present invention to provide an iterative decoder and iterative decoding method, in which the output of each component decoder is checked for the presence or absence of errors while decoding and which stops decoding immediately if no errors are detected, in a continuous mode

It is a sixth object of the present invention to provide an iterative decoder and iterative decoding method, in which the output of each component decoder is checked for the presence or absence of errors at the time when the output of the component decoder is arranged in the original order and stops decoding immediately if no errors are detected, in a continuous mode.

It is a seventh object of the present invention to provide an iterative decoder and iterative decoding method, in which, when each component decoder is operated in a continuous mode, one frame is subjected to an error check simultaneously with completion of decoding that one frame in a first component decoder and decoding is immediately stopped if no errors are detected.

Briefly, these and other objects are achieved by providing an iterative decoder. In the iterative decoder, a first adder has a first port for receiving information symbols and a second port; a first component decoder is coupled to the first adder, for receiving first parity symbols and decoding the information symbols using the first parity symbols and an output signal of the first adder; a first

subtractor has a third port for receiving the output of the first component decoder, and a fourth port; an interleaver coupled to the output of the second adder, for interleaving the decoded information symbols received from the first component decoder; a second component decoder receives the output of the interleaver and second parity symbols and decodes the information symbols of the interleaver output using the received signals; a deinterleaver deinterleaves the output of the second component decoder; a third adder has a fifth port for receiving the output of the deinterleaver and a sixth port for receiving an inversed output of the second adder, the output of the third adder connected to the second port and an inverted output of the third adder connected to the fourth port; a hard decision device converts the decoded symbols received from the first component decoder to binary information bits; an error detector checks error in the binary information bits received from the hard decision device and generates a no error signal if no errors are detected; and an output buffer stores the binary information bits received from the hard decision device and outputs the stored binary information bits in response to the no error signal.

In an iterative decoding method for an iterative decoder having a predetermined maximum number of iterations, including the steps of: iterative decoding an input frame signal; checking for errors in the decoded frame data before the predetermined number of iterations are completed; and outputting the decoded frame if no errors are detected.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of an iterative decoder with a code rate of 1/3 according to an embodiment of the present invention;

FIG. 2 is a block diagram of an error checker shown in FIG. 1 for describing its operation according to an embodiment of the present invention; and

FIG. 3 is a flowchart illustrating an iterative decoding method according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described hereinbelow with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

FIG. 1 is a block diagram of an iterative decoder with a code rate of 1/3 according to an embodiment of the present invention.

The first, second, and third input signals are signals demodulated and quantized by a demodulator (not shown) in a receiver (not shown). The first, second and third signals are a systematic signal X_k, a parity signal Y_{1k}, and another parity signal Y_{2k}, respectively. The second and third input signals are redundant values added to the original data for error correction, and are turbo-encoded and interleaved by a transmitter.

First and second component decoders 120 and 150, respectively, can operate in a continuous mode. RESOVA (Register Exchange Soft Output Viterbi Algorithm) decoders can be used as the first and second component decoders 130 and 150. For the input of each soft signal value of a group of bits such as a frame, the first and second component decoders 120 and 150 output each decoded soft signal value sequentially. In a continuous mode, the first and second component decoders 120 and 150 output one encoded soft signal value for one soft signal value input to the next end without delay, if as long a delay as an initial window size or decoding depth D is neglected. Each decoded soft signal value output from the first component decoder 120 is converted to a high or low value through hard decision by a level decider 185 and then applied to an error checker 190 without delay. The error checker 190 can be a CRC checker.

Due to the fact that the signal values flow without any delay, the error checker 190 completes an error check on one frame of soft signal values simultaneously when the first component decoder 120 completely decodes the

same one frame of soft signal values. That is, each decoded soft signal value output from the first component decoder 120 is converted to a high or low value through hard decision by the level decider 185 and is then applied to the error checker 190 bit by bit. The output of the level decider 185 is stored in an output buffer 195. In terms of the hardware, the first component decoder 120 outputs one decoded soft signal value at every clock count and feeds it to each register of the error checker 190 without any delay. Thus, the decoding of one frame in the first component decoder 120 is completed simultaneously with completion of an error check on the frame in the error checker 190.

If no errors are detected in the input frame, the error checker 190 stops the iterative decoding and outputs the one decoded frame stored in the output buffer 195. On the other hand, if errors are detected, the error checker 190 performs an error check again during decoding in the second component decoder 150. The iterative decoding can occur a predetermined number of times.

An adder 110 adds X_K to an extrinsic information signal EXT2 fed back from a second subtracter 170. EXT2 does not exist in initial decoding and is a signal component resulting from decoding in the second component decoder 150. From the input of the added signal (X_K + EXT2) from the first adder 110 and Y_{1K}, the first component decoder 120 outputs a primary decoded signal including X_K, EXT1, and EXT2 components. A first subtracter 130 subtracts the EXT2 component from the output of the first component decoder 120. Namely, the signal at node NA consists of X_K and EXT1 components. The level decider 185 converts the first component decoder 120 output signal (including X_K, EXT1, and EXT2 components) with data values in their original order, to high or low values through hard decision decoding and feeds the converted values to the error checker 190 without a delay.

An interleaver 140 permutes a bit sequence of the signal (X_K + EXT1) received from the first subtracter 130 by interleaving, and outputs an interleaved signal including X_K and EXT1 components. The second component decoder 150 decodes the output of the interleaver 140 and Y_{2K}, and outputs a secondary decoded signal including X_K, EXT1, and EXT2 components. A deinterleaver 160

rearranges the output of the second component decoder 150 in its original data order by deinterleaving. The second subtracter 170 subtracts the signal (X_K and EXT1) received from the node NA from the rearranged decoded soft signal including X_K, EXT1, and EXT2 components received from the deinterleaver 160. The difference signal is fed back as the extrinsic information signal EXT1 to the first adder 110.

After the deinterleaver 160 rearranges X_K in its original data order by deinterleaving the output of the second component decoder 150 as stated above, the error checker 190 can check errors in the output of the deinterleaver 160 received through a level decider 180.

As the above iterative decoding proceeds, soft signal values output from the first or second component decoder 120 or 150 generally have an improved error correction performance. The error checker 190 checks errors in the output of each component decoder until the output of one of the decoders is error-free at a certain time point. When this occurs, the error checker 190 stops the iterative decoding and the output buffer 195 outputs the error-free decoded signal. That is, if the decoded data is error-free before a prescribed number of decodings are completed, the iterative decoding is stopped, the error-free decoded data is output, and then the next frame is input.

In the iterative decoder shown in FIG. 1, the error check of each component decoder's output and decoding can occur at the same time without an additional processing delay in hardware. If no errors are detected in the check, the iterative decoding can be stopped immediately. Consequently, excess decoding is prevented, which, in turn, prevents the overuse of system resources and excess decoding-caused errors.

The deinterleaver 160 rearranges the output of the second decoder 150 in its original data order by deinterleaving prior to an error-check on the output of the second component decoder 150 in the error checker 190. Therefore, the error checker 190 can check errors in the output of the second component decoder 150 after a one frame-delay. The output of the iterative decoder is subjected to an

error check when it is arranged in its original data order.

FIG. 2 is a block diagram of the operation of the error checker 190 from FIG. 1 according to an embodiment of the present invention. Here, the error checker 190 is assumed to be a CRC error checker.

Referring to FIG. 2, the CRC error checker is composed of shift registers 232 to 238 serially connected. CRC polynomial coefficients G1 222 to G15 226 are preset to values of 0s or 1s. XOR gates 212 to 218 XOR-operates the coefficients and the outputs of the shift registers. When the clock count is 0, the first component decoder 120 has no output and the CRC error checker is inoperative. When the clock count is D, where D equals the decoding depth of the first component decoder 120, the CRC error checker CRC-checks the hard-decision output of the first component decoder 120, while shifting it bit by bit, as shown in FIG. 2. That is, the first component decoder outputs a signal value to a shift register at every clock count, and at the same time, the CRC error checker calculates a syndrome. Consequently, the CRC error checker can check errors in one frame simultaneously with the first component decoder completing decoding of the same frame.

For a detailed description of the operation of the CRC error checker, see "Error Control Coding: Fundamentals and Applications" Shu Lin and Daniel J. Costello Jr., Prentice Hall, p. 99.

FIG. 3 is a flowchart illustrating an iterative decoding method according to an embodiment of the present invention.

Referring to FIG. 3, the error checker 19 is initialized under the control of a controller in step 310. The initialization of the error checker 190 is equivalent to initialization of the shift registers. The controller sets the iteration count to 1 in step 320 and the first component decoder 120 decodes input soft values and outputs decoded soft values sequentially in step 330. At the same time, the error checker 190 receives the hard-decision output of the first component decoder 120 without a delay and checks errors in the received signal under the control of the controller.

Therefore, the decoding and the error check of one frame are completed at the same time in the first component decoder 120 and the error checker 190, respectively.

If the error checker 190 detects no errors in step 340, it stops the iterative decoding and outputs one decoded frame through the output buffer 195 under the control of the controller in step 390. On the other hand, if errors exist in step 340, the second component decoder 150 decodes the frame of soft signal values under the control of the controller and outputs the decoded soft signal values sequentially in step 350. The error checker 190 checks errors in the hard-decision deinterleaver output, that is, the output of the second component decoder 150 under the control of the controller. If no errors are generated in step 360, the error checker 190 performs step 390 under the control of the controller. If there are errors in step 360, the controller determines whether the current iteration count exceeds a maximum iteration value in step 370. If the former is greater than or equal to the latter, the controller deletes the contents of the output buffer 195. If not, the controller increments the iteration count by one in step 380 and returns to step 330.

In accordance with the iterative decoder and iterative decoding method according to an embodiment of the present invention as described above, iterative decoding is stopped immediately if a plurality of input signals are decoded without error and there is no processing delay is involved in the error check, thereby saving system resources.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS:

1. An iterative decoder comprising:

a first adder having a first port for receiving information symbols and a second port for receiving an extrinsic information signal EXT2;

a first component decoder for receiving first parity symbols, and for decoding the information symbols using the first parity symbols and an output signal of the first adder;

a first subtractor having a third port for receiving an output of the first component decoder, and a fourth port for receiving an inverted signal of the extrinsic information signal EXT2;

an interleaver coupled to an output of the first subtractor, for interleaving the decoded information symbols received from the first component decoder;

a second component decoder for receiving an output of the interleaver and second parity symbols, and for decoding the information symbols from the interleaver output using the received signals;

a deinterleaver for deinterleaving an output of the second component decoder;

a second subtractor having a fifth port for receiving an output of the deinterleaver and a sixth port for receiving an inverted output of the first subtractor, said third adder having output to the second port and inverted output to the fourth port;

a hard decision device for converting output received from the first component decoder to binary information bits by hard decision decoding;

an error detector for checking error in the binary information bits received from the hard decision device and for generating a no error signal if no errors are detected; and

an output buffer for storing the binary information bits received from the hard decision device and for outputting the stored binary information bits in response to the no error signal.

2. The iterative decoder of claim 1, wherein the first and second component decoders are operated in a continuous mode.

3. The iterative decoder of claim 1, wherein the error detector is a CRC (Cyclic Redundancy Code) error checker.

4. An iterative decoding device having a predetermined maximum number of iterations, comprising:

an iterative decoder for decoding an input frame signal and for outputting decoded frame data before the predetermined number of iterations are completed; and

an error detector for detecting errors in the decoded frame data received from the iterative decoder ;

wherein it is checked whether there are no errors in the decoded frame data, and if there are no errors, it makes for decoded frame data to be output.

5. The iterative decoding device of claim 4, wherein the decoded frame data is the output of at least one component decoder in the iterative decoder having two decoders.

6. The iterative decoding device of claim 4, wherein the error detector performs the error detection on the decoded frame data as the decoded frame is rearranged in the original data order.

7. The iterative decoding device of claim 5, wherein the error detector performs the error detection on the decoded frame data of a first component decoder of the iterative decoder.

8. The iterative decoding device of claim 4, wherein the iterative decoder comprises:

a first adder having a first port for receiving information symbols and a second port for receiving an extrinsic information signal EXT2;

a first component decoder, for receiving first parity symbols, and for decoding the information symbols using the first parity symbols and an output signal of the first adder;

a first subtractor having a third port for receiving an output of the first component decoder, and a fourth port for receiving an inverted signal of the

extrinsic information signal EXT2;

an interleaver coupled to an output of the first subtractor, for interleaving the decoded information symbols received from the first component decoder;

a second component decoder for receiving an output of the interleaver and second parity symbols, and for decoding the information symbols from the interleaver using the received signals;

a deinterleaver for deinterleaving an output of the second component decoder; and

a second subtractor having a fifth port for receiving an output of the deinterleaver and a sixth port for receiving an inverted output of the second adder, said second subtractor having output to the second port and inverted output to the fourth port.

9. The iterative decoding device of claim 8, wherein the error detector performs the error detection on the output of the first component decoder.

10. The iterative decoding device of claim 8, wherein the first and second component decoders are operated in a continuous mode.

11. The iterative decoding device of claim 8, wherein the error detector is a cyclic redundancy code (CRC) error checker.

12. The iterative decoding device of claim 8, wherein the error detector performs the error detection on the output of the deinterleaver.

13. The iterative decoding device of claim 8, wherein the error detector receives the output of one of the first component decoder and the deinterleaver, and performs error detection on each output.

14. An iterative decoding method for an iterative decoder having a predetermined maximum number of iterations, comprising the steps of:

iterative decoding an input frame signal;

checking for errors in the decoded frame data before the predetermined number of iterations are completed; and

outputting the decoded frame if no errors are detected.

15. The iterative decoding method of claim 14, wherein the decoded frame data is the output of at least one component decoder in the iterative decoder.

16. The iterative decoding method of claim 15, wherein the error checking is performed on the decoded frame data as the decoded frame is rearranged in the original data order.

17. The iterative decoding method of claim 15, wherein the error checking is performed on the decoded frame data of a first component decoder of the iterative decoder.

18. The iterative decoding method of claim 14, wherein the steps by the iterative decoder comprises:

adding information symbols and an extrinsic information signal EXT2;

first-decoding the information symbols using a first parity symbols and information symbols to which the extrinsic information signal EXT2 is added.

subtracting the first-decoded information symbols and an inverted signal of the extrinsic information signal EXT2;

interleaving the first-decoded information symbols to which the inverted signal of the extrinsic information signal EXT2 is subtracted;

performing a second-decoding using the interleaved information symbols and a second parity symbols; and

deinterleaving the second-decoded information symbols.

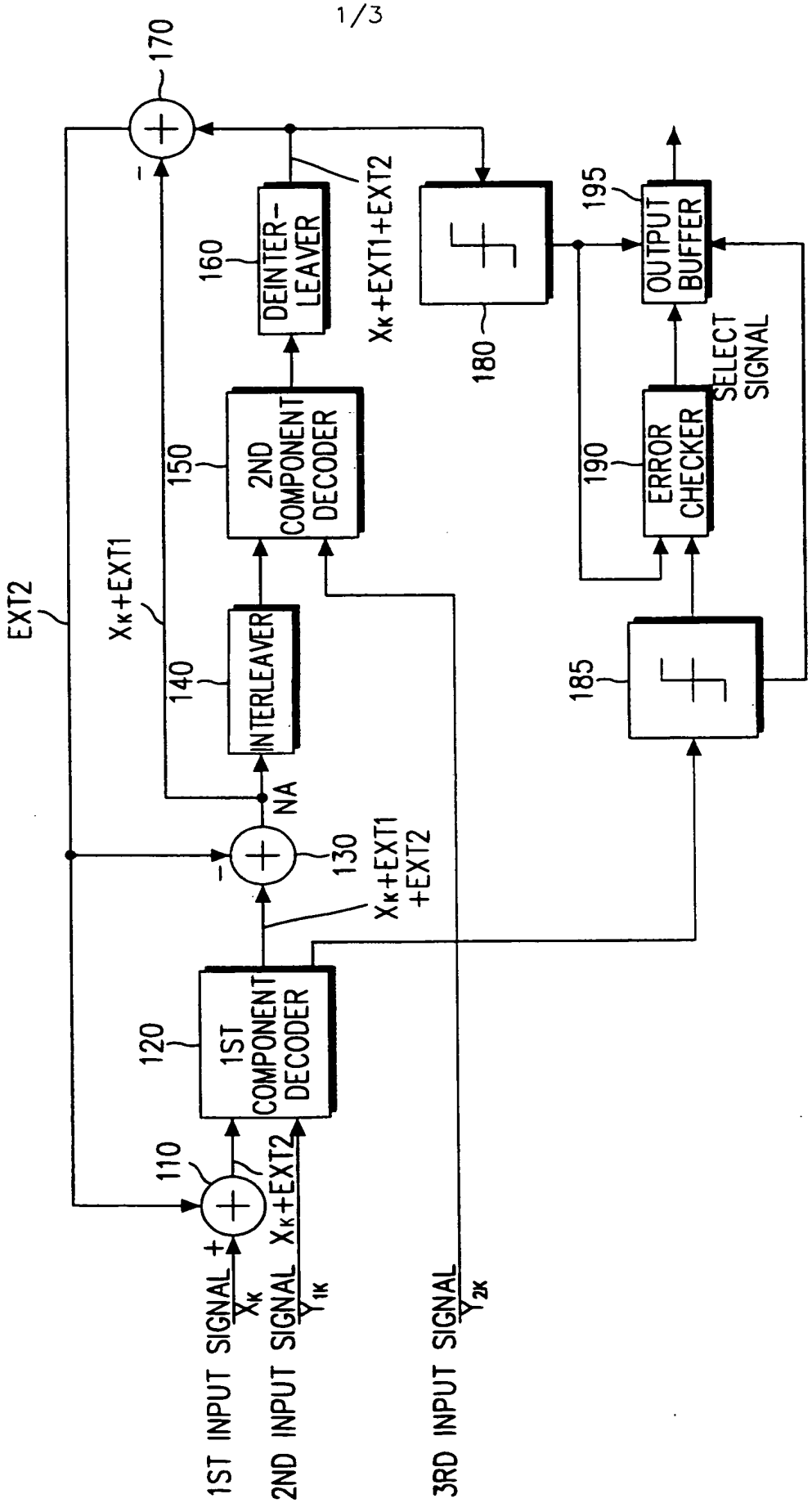
19. The iterative decoding method of claim 18, wherein the error checking is performed on the output of the first component decoder.

20. The iterative decoding method of claim 18, wherein the first and second component decoders are operated in a continuous mode.

21. The iterative decoding method of claim 18, wherein the error checking is performed on a Cyclic Redundancy Code (CRC) error.

22. The iterative decoding method of claim 18, wherein the error checking is performed on the output of the deinterleaver.

FIG.1



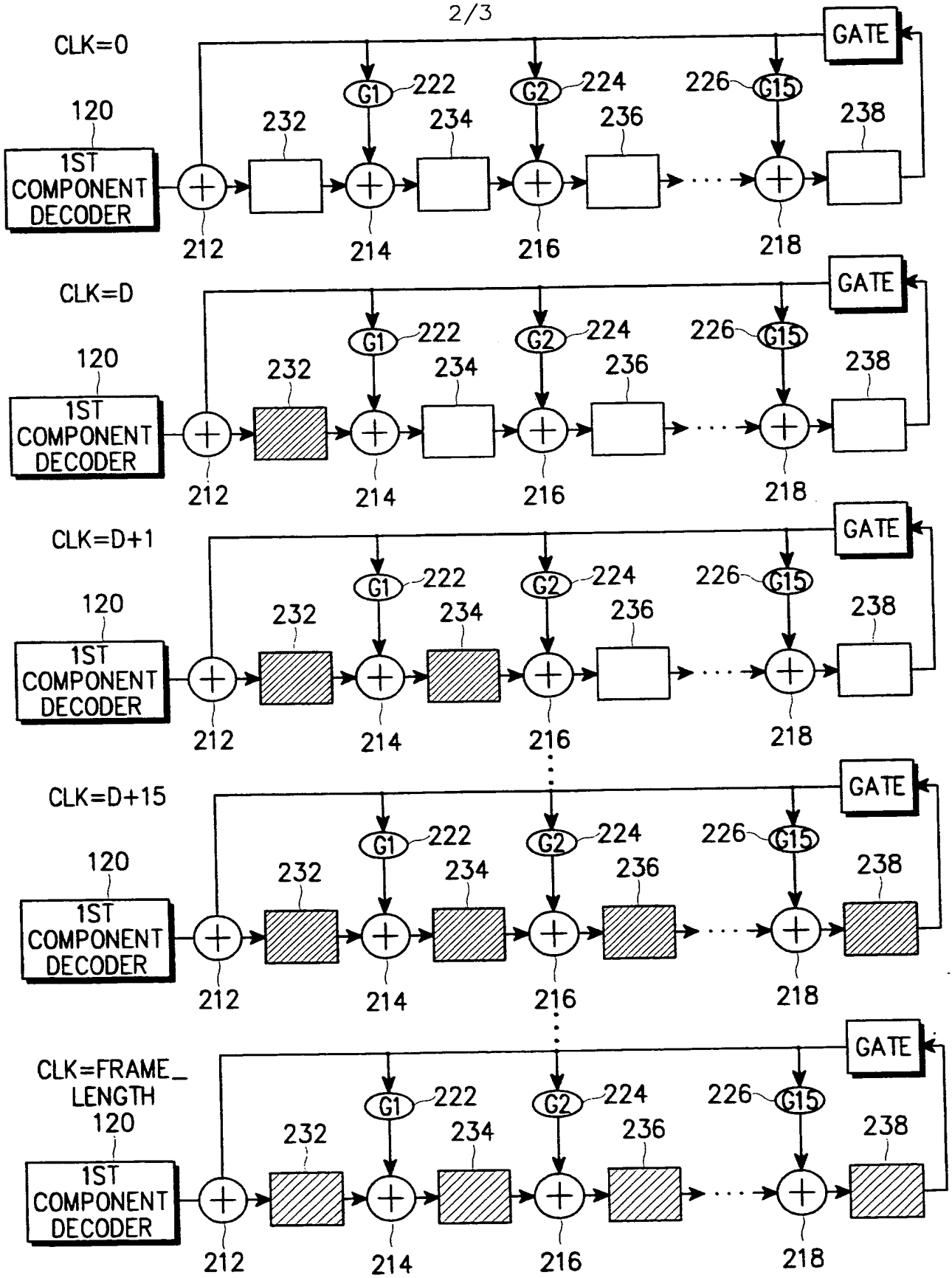

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FIG.2

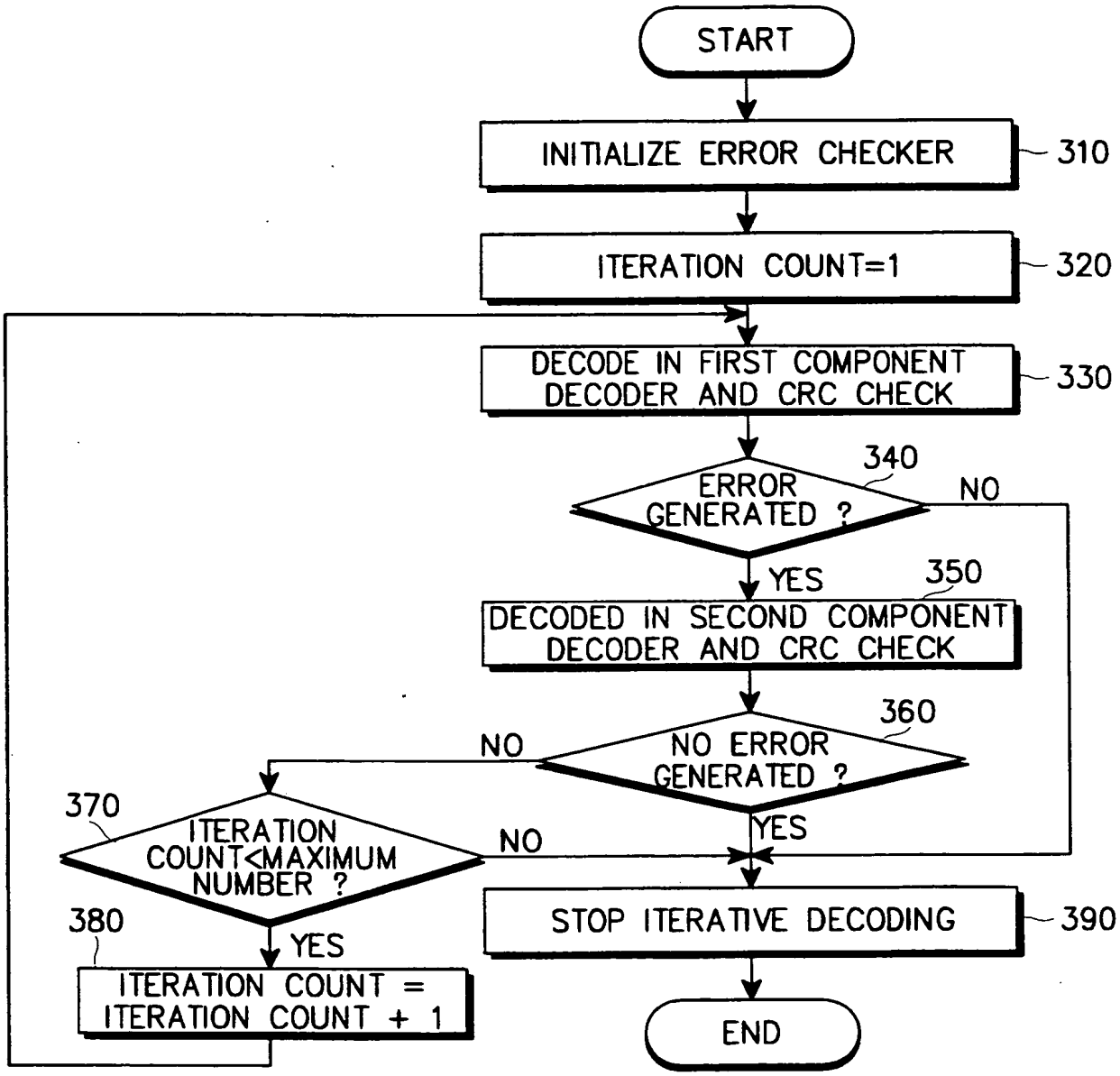

FIG.3

INTERNATIONAL SEARCH REPORT

international application No.
PCT/KR99/00844

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H03M 7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimun documentation searched (classification system followed by classification symbols)

IPC 7 H03M G11B

Documentation searched other than minimun documentation to the extent that such documents are included in the fileds searched

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Electronic data base consulted during the internationl search (name of data base and, where practicable, search trerms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4271520 A (MOTOROLA, INC.) 02 June 1981 page 3, line 53 - page 4, line 27	1, 4
Y	KR 98-703844 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 05 December 1998 page 15, line 16 - line 26	1
Y	KR 203722 B (AT&T) 24 March 1999 page 13, line 7 - line 20, claim 16	4
A	EP 0551973 A (AMPEX CORPORATION) 21 JULY 1993 see fig 2	1, 4

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 APRIL 2000 (12.04.2000)	14 APRIL 2000 (14.04.2000)

Name and mailing address of the ISA/KR	Authorized officer
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